09/855241

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Vinodh R. Cuppu, et al.   Docket: 14138

Patent No.:   6,948,051 B2   Dated: November 14, 2005

Issued: September 20, 2005

For: METHOD AND APPARATUS FOR REDUCING LOGIC
ACTIVITY IN A MICROPROCESSOR USING REDUCED
BIT WIDTH SLICES THAT ARE ENABLED OR DISABLED
DEPENDING ON OPERATION WIDTH

Certificate
NOV 2 1 2005
of Correction

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Sir:

It appears that errors have been introduced in the course of printing

the Patent issued in the above application, and it is respectfully requested that the

Commissioner issue a Certificate of Correction in the following respects:

[75] Inventors:
"Jude A. Rivers, Cortland Manor, NY" should read -- Jude A. Rivers, Peekskill, NY --

[75] Inventors:
Vinodh R. Cuppu, Fairfax, VA" should read -- Vinodh R. Cuppu, McLean, VA --

Column 6, Line 18:
"Missing ¶" should read -- Figure 8 illustrates the width determination WD logic expanded
to show overflow detection, as explained in greater detail
hereinbelow --

NOV 2 2 2005

Column 6, Line 18:
"lookup of the REtags" should read -- lookup of the RFtags --

Column 7, Line 33:
"indicates the WED" should read -- indicates the WD --

Column 8, Line 41,42:
"=X"00000000" should read -- X"0000 _ 0000 --

Column 8, Line 44:
"(X"0000 00" should read -- (X"0000 _ 00 --

Column 8, Line 44:
"X"Ffff Ff" should read -- X"Ffff_Ff --

Column 10, Line 8:
"determinations;" should read -- determinations: --

<div align="right">

Respectfully submitted,

Steven Fischman
Reg. No. 34,594

</div>

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO   : **6,948,051** *B2*

APPLICATION NO : **09/855,241**

ISSUE DATE   : **September 20, 2005**

INVENTOR(S)   : **Vinodh R. Cuppu, et al.**

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

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